I claim:

1. An apparatus comprising:

a tag array to store address information for data blocks;

a data array to store data blocks;

a decoder to access first and second entries of the tag array responsive to a request; and

hit/miss logic to process the request, responsive to hit/miss signals triggered by the access to the first and second entries.

2. The apparatus of claim 1, wherein the data blocks are instruction blocks, the request specifies a target address for an instruction block, and the first and second entries correspond to an entry to which a portion of the target address maps and an adjacent entry, respectively.

3. The apparatus of claim 2, wherein the hit/miss logic triggers a request to a higher-level cache if the access to the first entry of the tag array misses.

4. The apparatus of claim 2, wherein the hit/miss logic signals the higher-level cache to return a full cache line if the accesses to the first and second entries both miss.

5. The system of claim 4, wherein the hit/miss logic signals the higher-level cache to return a partial cache line if the access to the first entry misses and the access to the second entry hits.

6. The system of claim 1, wherein the tag array includes first and second tag ports to process the first and second accesses.

7. The system of claim 6, wherein the data array includes a first data port to process a first access that hits in the tag array, the first tag and data arrays forming a standard port.

8. The system of claim 7, wherein the decoder drives a first index to the first tag port and drives a modified version of the first index to the second tag port.

9. A method comprising:

detecting a target address;

generating first and second look-ups to a cache responsive to the target address; and

retrieving a data block from a second cache responsive to hit/miss signals generated by the first and second look-ups.

10. The method of claim 9, wherein generating comprises:

determining a first index from a first portion of the target address;

determining a second index from the first index; and

generating the first and second look-ups to entries indicated by the first and second indices, respectively.

11. The method of claim 9, wherein retrieving comprises retrieving a data block from the second cache responsive to the first look-up missing in the first cache.

12. The method of claim 11, wherein retrieving a data block comprises:

retrieving a data block having a first size responsive to the second look-up hitting in the first cache; and

retrieving a data block having a second size responsive to the second look-up missing in the first cache.

13. The method of claim 9, wherein generating first and second look-ups comprises:

generating a standard look-up to a first set determined from a portion of the target address; and

generating a pseudo-look-up to second set adjacent to the first set.

14. A device comprising:

a first cache including a plurality of entries, each entry to store an instruction block having a first size;

a decoder to generate multiple look-ups to the first cache responsive to a target address;

a second cache including a plurality of entries, each entry to store an instruction block having a second size that is greater than the first size; and

a request manager to transfer to the first cache an instruction block from the second cache having one of a plurality of sizes, responsive to results of the primary and secondary look-ups.

15. The device of claim 14, wherein the multiple look-ups are primary and secondary look-ups and the request manager transfers an instruction block having the second size responsive to the primary and secondary look-ups missing in the first cache.

16. The device of claim 14, wherein the multiple look-ups are primary and secondary look-ups and the decoder generates first and second set indices for the primary and secondary look-ups, respectively, responsive to set bits of the target address.

17. The device of claim 15, wherein the first set index is derived from the set bits and the second set index is derived from the first set index.

18. The device of claim 14, wherein all of the multiple look-ups are processed if the target address meets a first criterion.

19. The device of claim 18, wherein the first criterion is that the target address maps to a boundary of the instruction block of the second cache.

20. The device of claim 18, wherein only a first of the multiple look-ups is processed if the target address does not meet the first criterion.

21. The device of claim 14, wherein the multiple look-ups comprise primary and secondary look-ups and the first cache includes a standard port to process the primary look-up and a pseudo-port to process the secondary look-up.

22. The device of claim 21, wherein the standard port comprises a tag port and a data port and the pseudo port comprises a tag port.

23. The device of claim 21, wherein the decoder drives a first index on the standard port and a second index, derived from the first index, on the pseudo port.

24. A computer system comprising:

a thread control unit to schedule execution of instructions from multiple threads;

an execution module to execute the scheduled instructions; and

a memory hierarchy to supply the execution module with instructions for the multiple threads, the memory hierarchy including:

a first cache to store instruction in multiple cache lines of a first size;

a second cache to store instructions in multiple cache lines of a second size that is different from the first size;

a main memory; and

a cache controller to generate multiple look-ups to the first cache responsive to an instruction address and to transfer a block of instructions to the first cache responsive to hit/miss signals generated by the multiple look-ups.

25. The system of claim 24, wherein the cache controller transfers a block of instructions to the first cache if a first of the multiple look-ups misses in the first cache, the block of instructions having a size equal to a portion of the cache line size of the second cache responsive to a hit/miss signal of another of the multiple look-ups.

26. The system of claim 25, further comprising a memory controller, wherein the memory controller transfers instructions from the main memory responsive to a miss in the second cache controller